

## U.S. APPLICATION NO. (if known, see 37 CFR 1.5)

U.S. APPLICATION NO. (If known, see 37 C.F.R. § 1.51(b))

PRIORITY DATE CLAIMED  
30 September 1999

## CONTROL LOOP FOR DIGITAL SIGNALS

Andreas MENKHOFF

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
3. ☐ This is an express request to begin national examination procedures (35 U.S.C. 371(f)). The submission must include items (5), (6), (9) and (21) indicated below.
4. ☐ The US has been elected by the expiration of 19 months from the priority date (Article 31).
5. ☒ A copy of the International Application as filed (35 U.S.C. 371(c)(2))
  - a. ☒ is attached hereto (required only if not communicated by the International Bureau).
  - b. ☐ has been communicated by the International Bureau.
  - c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US).
6. ☐ An English language translation of the International Application as filed (35 U.S.C. 371(c)(2)).
  - a. ☐ is attached hereto.
  - b. ☐ has been previously submitted under 35 U.S.C. 154(d)(4).
7. ☐ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371(c)(3))
  - a. ☐ are attached hereto (required only if not communicated by the International Bureau).
  - b. ☐ have been communicated by the International Bureau.
  - c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
  - d. ☐ have not been made and will not be made.
8. ☐ An English language translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371 (c)(3)).
9. ☐ An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)).
10. ☐ An English language translation of the annexes of the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371(c)(5)).

**Items 11 to 20 below concern document(s) or information included:**

11. ☒ An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
12. ☐ An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
13. ☐ A FIRST preliminary amendment.
14. ☐ A SECOND or SUBSEQUENT preliminary amendment.
15. ☐ A substitute specification.
16. ☐ A change of power of attorney and/or address letter.
17. ☐ A computer-readable form of the sequence listing in accordance with PCT Rule 13ter.2 and 35 U.S.C. 1.821 - 1.825.
18. ☐ A second copy of the published international application under 35 U.S.C. 154(d)(4).
19. ☐ A second copy of the English language translation of the international application under 35 U.S.C. 154(d)(4).
20. ☐ Other items or information:

U.S. APPLICATION NUMBER (SEE 37 CFR 1.53) <b>10/089654</b>		INTERNATIONAL APPLICATION NO. PCT/EP 00/09454		ATTORNEY'S DOCKET NUMBER Micronas.6581	
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21. <input checked="" type="checkbox"/> The following fees are submitted: <b>BASIC NATIONAL FEE (37 CFR 1.492 (a) (1) - (5)):</b> Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO and International Search Report not prepared by the EPO or JPO ..... <b>\$1040.00</b>  International preliminary examination fee (37 CFR 1.482) not paid to USPTO but International Search Report prepared by the EPO or JPO ..... <b>\$890.00</b>  International preliminary examination fee (37 CFR 1.482) not paid to USPTO but international search fee (37 CFR 1.445(a)(2)) paid to USPTO ..... <b>\$740.00</b>  International preliminary examination fee (37 CFR 1.482) paid to USPTO but all claims did not satisfy provisions of PCT Article 33(1)-(4) ..... <b>\$710.00</b>  International preliminary examination fee (37 CFR 1.482) paid to USPTO and all claims satisfied provisions of PCT Article 33(1)-(4) ..... <b>\$100.00</b>  <b>ENTER APPROPRIATE BASIC FEE AMOUNT =</b>			<b>CALCULATIONS PTO USE ONLY</b>          <div style="border: 1px solid black; padding: 2px;">\$ 890.00</div>		
Surcharge of <b>\$130.00</b> for furnishing the oath or declaration later than <input type="checkbox"/> 20 <input checked="" type="checkbox"/> 30 months from the earliest claimed priority date (37 CFR 1.492(e)).			<div style="border: 1px solid black; padding: 2px;">\$ 130.00</div>		
CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE	\$	
Total claims	- 20 =		x <b>\$18.00</b>	\$	
Independent claims	- 3 =		x <b>\$84.00</b>	\$	
MULTIPLE DEPENDENT CLAIM(S) (if applicable)			+ <b>\$280.00</b>	\$	
<b>TOTAL OF ABOVE CALCULATIONS =</b>				<b>\$1020.00</b>	
<input type="checkbox"/> Applicant claims small entity status. See 37 CFR 1.27. The fees indicated above are reduced by 1/2.				\$	
<b>SUBTOTAL =</b>				\$	
Processing fee of <b>\$130.00</b> for furnishing the English translation later than <input type="checkbox"/> 20 <input checked="" type="checkbox"/> 30 months from the earliest claimed priority date (37 CFR 1.492(f)).				<div style="border: 1px solid black; padding: 2px;">\$130.00</div>	
<b>TOTAL NATIONAL FEE =</b>				<b>\$1150.00</b>	
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31). <b>\$40.00</b> per property +				\$	
<b>TOTAL FEES ENCLOSED =</b>				<b>\$1150.00</b>	
				<b>Amount to be refunded:</b>	\$
				<b>charged:</b>	\$

a. ☒ A check in the amount of \$ 1150.00 to cover the above fees is enclosed.

b. ☐ Please charge my Deposit Account No. 13-1375 in the amount of \$ \_\_\_\_\_ to cover the above fees.  
A duplicate copy of this sheet is enclosed.

c. ☒ The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any  
overpayment to Deposit Account No. 19-0079. A duplicate copy of this sheet is enclosed.

d. ☐ Fees are to be charged to a credit card. **WARNING:** Information on this form may become public. **Credit card  
information should not be included on this form.** Provide credit card information and authorization on PTO-2038.

**NOTE:** Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137 (a) or (b)) must be filed and granted to restore the application to pending status.

SEND ALL CORRESPONDENCE TO:

Patrick J. O'Shea  
 Samuels, Gauthier & Stevens, LLP  
 225 Franklin Street  
 Suite 3300  
 Boston, MA 02110

*Patrick O'Shea*

 SIGNATURE  
 Patrick J. O'Shea  
 NAME

The PTO did not receive the following  
 listed item(s) \_\_\_\_\_

35,309

  
 REGISTRATION NUMBER

No Check Received

10089654 092402

**10/089654**

**IC10 Rec'd PCT/PTO 01 APR 2002**

Docket No: Mic.6581

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

**APPLICANT:** Andreas Menkhoff

**GROUP:** Not yet assigned

**INTERNATIONAL  
APPLN. NO.:** PCT/EP00/09454

**EXAMINER:** Not yet assigned

**SERIAL NO:** Not yet assigned

**INTERNATIONAL  
FILING DATE:** September 27, 2002

**FOR:** CONTROL LOOP FOR DIGITAL SIGNALS

**Box PCT  
Assistant Commissioner of Patents  
Washington, D.C. 20231**

**Sir:**

**CERTIFICATE OF EXPRESS MAIL UNDER 37 C.F.R. §1.10**

I hereby certify that the attached Transmittal Letter (PTO-1390) and the items referred to as being enclosed therewith are being deposited with the United States Postal Service on this date April 1, 2002 in an envelope as "Express Mail Post Office to Addressee" Mailing Label Number EV075028020US addressed to the Assistant Commissioner of Patents, Washington, D.C. 20231.



Christie A. Mims

Rec'd PCT/PTO 24 SEP 2002  
10/089,654  
Micronas. 6581  
10/089,654  
#5

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

**APPLICANT:** Andreas Menkhoff **GROUP:** Not yet assigned  
**INTERNATIONAL**  
**APPLN. NO.:** PCT/EP00/09454 **EXAMINER:** Not yet assigned  
**SERIAL NO:** 10/089,654  
**INTERNATIONAL**  
**FILING DATE:** 27 September 2000  
**FOR:** CONTROL LOOP FOR DIGITAL SIGNALS

**FIRST PRELIMINARY AMENDMENT**

Entry of this preliminary amendment is respectfully requested to remove the multiple dependent claims following the translation of the claims to English.

Please amend the application as follows:

IN THE CLAIMS:

Amend claims 3, 6 and 7 as follows:

3.(amended) Control loop according to Claim 2, characterized in that a multiplication unit (7) is connected between the integrator element (3) and the second multiplication element (5) for the multiplication of the integrating circuit input signal by a constant factor (K).

6.(amended) Control loop according to Claim 5, characterized in that the multiplication unit (7; 10) is made as a shift register.

7.(amended) Control loop according to Claim 5, characterized in that the constant factor (K) exhibits a value in the buildup phase of the control loop that is different from the value in the steady state.

Micronas.6581  
10/089,654

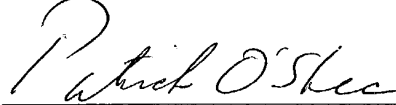
**REMARKS**

Claims 3, 6 and 7 have been amended. Claims 1-7 remain.

Examination on the merits is respectfully requested.

If a telephone interview could assist in the prosecution of this application, please call the undersigned attorney.

Respectfully submitted,



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Patrick J. O'Shea  
Registration No. 35,305  
Samuels, Gauthier & Stevens LLP  
225 Franklin Street, Suite 3300  
Boston, Massachusetts 02110  
Telephone: (617) 426-9180 x121

**VERSION WITH MARKINGS TO SHOW CHANGES MADE TO CLAIMS**

Amend claims 3, 6 and 7 as follows:

3.(amended) Control loop according to Claim ~~1 or 2~~, **characterized in that** a multiplication unit (7) is connected between the integrator element (3) and the second multiplication element (5) for the multiplication of the integrating circuit input signal by a constant factor (K).

6.(amended) Control loop according to ~~one of Claims 3 or 5~~, **characterized in that** the multiplication unit (7; 10) is made as a shift register.

7.(amended) Control loop according to ~~one of Claims 3 or 5~~, **characterized in that** the constant factor (K) exhibits a value in the buildup phase of the control loop that is different from the value in the steady state.

## Specification

## Control Loop for Digital Signals

This invention relates to a control loop in which an input signal is converted, by multiplication by an integrator value, to an output signal that exhibits on average a constant reference value.

Such control loops are used, for example, as so-called AGC (automatic gain control) circuits for the automatic gain adaptation of digital signals. In automatic gain control, from an input signal, an output signal having a constant time-average value, whose level is as a rule adjustable and independent of the level of the input signal, is generated.

In detector circuits for high-frequency signals, the AGC is used to furnish, for further signal processing, an intermediate signal whose time-average level is constant, independently of the field strength of the detected signal of the input stage.

A known control loop for digital signals is illustrated in Figure 1. The energy of an output signal OUT exhibits on average a constant value that can be set via a reference value REF. High-energy input signals thus must be diminished in amplitude and low-energy input signals must be augmented in amplitude.

The output signal OUT is first adapted in a signal converter 1 in such a fashion that it can be compared to the reference value REF. If the output signal OUT is, for example, an electric current, then a voltage proportional to the current is derived to the signal converter and then compared to a

reference voltage. Signal converter 1 can also adapt the output signal OUT in such a fashion that the control behavior of the control loop is as favorable as possible. Signal-processing functions such as for example magnitude formation, squaring, or calculation of the distortion factor are suitable for this purpose. If one of the cited signal-processing functions is selected, it is guaranteed that only positive values are employed for the comparison even in case of a negative output signal OUT.

The comparison itself includes taking a difference with a difference element 2, in which the adapted output signal OUT is subtracted from the reference value REF. The difference element 2 supplies a difference  $\Delta IN$ . The difference  $\Delta IN$  is fed to an integrator element 3, which determines an integrator value IW therefrom. Integrator element 3 cumulates the difference  $\Delta IN$ . If the difference  $\Delta IN$  is positive, the integrator value IW is increased; if the difference  $\Delta IN$  is negative, it is decreased. In a multiplication element 4, the input signal IN is multiplied by the integrator value IW. The result of this multiplication is the output signal OUT.

The circuit of Figure 1 can be described mathematically by

$$\Delta IN = REF - IN * IW.$$

In the steady-state condition, that is, when the control loop has built up to a steady state,  $\Delta IN = 0$ . Hence it follows that

$$\Delta IN = REF - IN * IW = 0 \text{ or, after manipulation,} \\ IW = REF/IN.$$

Hence, finally, one obtains the desired output value OUT as

$$OUT = IN * IW = IN * REF/IN = REF.$$

The disadvantage of this circuit is the long buildup time that is required if the energy of the input signal IN



deviates substantially from the reference value REF. In case of a large deviation, several hundred cycles are required to set the reference value REF exactly. This long buildup time is not acceptable in time-critical control tasks.

It is a goal of the present invention to identify a control loop for the conversion of an input signal, by multiplication by an integrator value, into an output signal that exhibits on average a constant reference value, which control loop exhibits improved control behavior as a consequence of a simple supplementary circuit. This goal is achieved with a control loop having the features of Claim 1. This goal is also achieved with a control loop having the features of Claim 4.

The invention has the advantage that the control behavior of the known control loop can be improved substantially with only a minor supplementary circuit. The individual components of the known control loop can continue to be used.

It is especially advantageous that the multiplication units and the division element can be implemented with simple shift registers (barrel shifters) if the constant factor or the reference value can be represented as a power of 2.

Advantageous further embodiments are characterized in dependent claims.

In what follows, the invention is explained in more detail on the basis of exemplary embodiments illustrated in the figures of the drawing. Corresponding elements are identified by the same reference numerals. The figures show:

Figure 1: a known control loop;

Figure 2: a control loop according to the invention having additional feedback;

Figure 3: a control loop according to the invention with counter.

According to a first exemplary embodiment according to Figure 2, a difference element 2 has its output connected to a first multiplication element 5. Difference element 2 exhibits inputs for a reference value REF and an output signal OUT. Before it is fed to difference element 2, the output signal OUT can be adapted by a signal converter 1 to the reference value REF with respect to the physical unit. Difference element 2 forms the difference from the reference signal REF and the output signal OUT and passes this on to first multiplication element 5. This multiplies the difference  $\Delta IN$  by a weighting factor GF. The result is passed on to an integrator element 3. Integrator element 3 integrates the difference  $\Delta IN$  weighted with the weighting factor GF. The result of this integration is forwarded by integrator element 3 to a second multiplication element 4 as the integrator value IW. In second multiplication element 4, an input signal IN is multiplied by the integrator value IW. The result of this multiplication of second multiplication element 4 represents the output signal OUT.

The weighting factor GF is derived from the integrator value IW and fed back via first multiplication element 5 to integrator element 3. Favorable control behavior results if the integrator value IW is not used directly as weighting factor GF. It is more favorable to divide the integrator value IW by the reference value REF and weight the difference  $\Delta IN$  therewith. The weighting factor GF in this case is the quotient of the integrator value IW and the reference value REF. A division element 6 is provided for the performance of this division IW/REF. A first input of division element 6 is connected to an output of integrator element 3 in order to feed the integrator value IW to division element 6. A second input of division element 6 is connected to an input of difference

According to a second exemplary embodiment according to Figure 3, difference element 2 again has its output connected to integrator element 3. Difference element 2 subtracts from the reference value REF the output signal OUT, which may be adapted in signal converter 1, and forwards the difference  $\Delta IN$  to integrator element 3. In this exemplary embodiment, integrator element 3 can take on only values between a lower

and an upper threshold. If the integrator value already lies near the upper threshold, subsequent integration takes place near the lower threshold. If the integrator value  $IW$  lies near the lower threshold, then in case of a further decrease below the lower threshold, counting continues near the upper threshold. Integrator element 3 thus exhibits an overflow and an underflow. Along with the integrator value  $IW$ , there is at a carry output  $UA$  a count signal, which passes on any passage beyond one of the thresholds to a counter 8. The counter increments its count in case of overflow and decrements the count in case of underflow. Counter 8 has its output connected to an input multiplication element 9. Input multiplication element 9 multiplies the input signal  $IN$  by the count, which represents the number of passages beyond the lower and upper threshold. The result of this multiplication is fed to second multiplication element 4, which multiplies it by the integrator value  $IW$  in order to obtain the output signal  $OUT$ .

With the exemplary embodiment according to Figure 3, the input signal  $IN$  is scaled with a scaling factor. The scaling factor is  $2^n$ , where  $n$  corresponds to the count of counter 8. In case of large deviations of the input signal  $IN$  from the reference value  $REF$ , the scaling brings the input signal to the order of magnitude of the reference value. Thus it is guaranteed that the ratio of integrator value to reference value lies near 1.

A further improvement of the control behavior is achieved if an intermediate multiplication element 10 is provided between integrator element 3 and difference element 2. The difference  $\Delta IN$  is weighted with this by the factor  $K$ .

## Claims

1. Control loop for the conversion of an input signal (IN), by multiplication by an integrator value (IW), to an output signal (OUT) that exhibits on average a constant reference value (REF), having

- a first multiplication element (4) for multiplication of the input signal (IN) by the integrator value (IW)
- a difference element (2) for formation of a difference between the output signal (OUT) and the reference value (REF) and
- an integrator element (3) for the formation of the integrator value (IW) from an integrator input signal,

**characterized in that** a second multiplication element (5) is provided between the difference element (2) and the integrator element (3) for the formation of the integrator input signal from the difference weighted with a weighting factor (GF) derived from the integrator value (IW).

2. Control loop according to Claim 1,

**characterized in that** a division element (6) is provided for the calculation of the weighting factor (GF) by division of the integrator value (IW) by the reference value (REF).

3. Control loop according to Claim 1 or 2,

**characterized in that** a multiplication unit (7) is connected between the integrator element (3) and the second multiplication element (5) for the multiplication of the integrating circuit input signal by a constant factor (K).

4. Control loop for the conversion of an input signal (IN), by multiplication by an integrator value (IW), to an output signal (OUT) that exhibits on average a constant reference value (REF), having

- a multiplication element (4) for the multiplication of the input signal (IN) by the integrator value (IW)
- a difference element (2) for the formation of a difference between the output signal (OUT) and the reference value (REF) and
- an integrator element (3) for the formation of the integrator value (IW) from an integrator input signal,

**characterized in that** a multiplication unit (9) is provided for the scaling of the input signal (IN) with a value determined by a counter (8), which is connected to an output (UA) of the integrator element (3) and counts the number of passages of the integrator value (IW) beyond a lower and an upper threshold, the multiplication unit and the multiplication element being connected in series.

5. Control loop according to Claim 4,

**characterized in that** a further multiplication unit (10) is connected between the integrator element (3) and the difference element (2) for the multiplication of the integrating circuit input signal by a constant factor (K).

6. Control loop according to one of Claims 3 or 5,

**characterized in that** the multiplication unit (7; 10) is made as a shift register.

7. Control loop according to one of Claims 3 or 5,

**characterized in that** the constant factor (K) exhibits a value in the buildup phase of the control loop that is different from the value in the steady state.

(12) NACH DEM VERTRAG FÜR DIE INTERNATIONALE ZUSAMMENARBEIT AUF DEM GEBIET DES  
PATENTWESENS (PCT) VERÖFFENTLICHTE INTERNATIONALE ANMELDUNG

(19) Weltorganisation für geistiges Eigentum  
Internationales Büro



(43) Internationales Veröffentlichungsdatum  
5. April 2001 (05.04.2001)

PCT

(10) Internationale Veröffentlichungsnummer  
**WO 01/24360 A1**

(51) Internationale Patentklassifikation<sup>7</sup>: H03G 3/00

(74) Anwalt: WESTPHAL MUSSGNUG & PARTNER;  
Mozartstrasse 8, D-80336 München (DE).

(21) Internationales Aktenzeichen: PCT/EP00/09454

(81) Bestimmungsstaat (national): US.

(22) Internationales Anmeldedatum:  
27. September 2000 (27.09.2000)

(84) Bestimmungsstaaten (regional): europäisches Patent (AT,  
BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC,  
NL, PT, SE).

(25) Einreichungssprache: Deutsch

(26) Veröffentlichungssprache: Deutsch

Veröffentlicht:

— Mit internationalem Recherchenbericht.

(30) Angaben zur Priorität:  
199 47 048.0 30. September 1999 (30.09.1999) DE

(71) Anmelder (für alle Bestimmungsstaaten mit Ausnahme  
von US): MICRONAS MUNICH GMBH [DE/DE];  
Balanstrasse 73, 81541 München (DE).

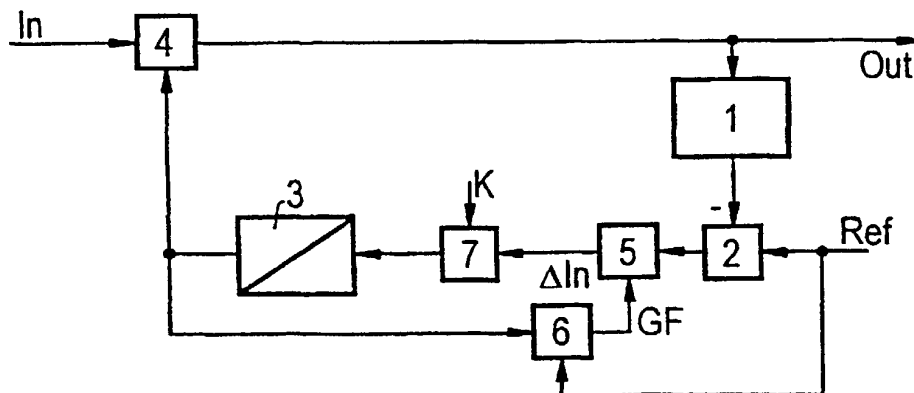
Zur Erklärung der Zweibuchstaben-Codes, und der anderen  
Abkürzungen wird auf die Erklärungen ("Guidance Notes on  
Codes and Abbreviations") am Anfang jeder regulären Ausgabe  
der PCT-Gazette verwiesen.

(72) Erfinder; und

(75) Erfinder/Anmelder (nur für US): MENKHOFF, An-  
dreas [DE/DE]; Höslstrasse 17, 81927 München (DE).

(54) Title: CONTROL LOOP FOR DIGITAL SIGNALS

(54) Bezeichnung: REGELKREIS FÜR DIGITALE SIGNALE



(57) Abstract: The invention improves the control behavior of a control circuit for digital signals which is used in AGCs (automatic gain control), using a simple supplementary circuit. In a first example of an embodiment, the output signal of an integrator member is looped back to the input of said integrator member in the loop-back branch of the control circuit. In a second example, a counter is provided. Said counter monitors the overflow of the integrator member and weights the input signal accordingly.

(57) Zusammenfassung: Die Erfindung verbessert das Regelverhalten eines Regelkreises für digitale Signale, der in AGCs (automatic gain control) eingesetzt wird, mit Hilfe einer einfachen Zusatzbeschaltung. Bei einem ersten Ausführungsbeispiel wird das Ausgangssignal eines Integrierergliedes im Rückkopplungsweig des Regelkreises auf den Eingang des Integrierergliedes zurückgekoppelt. Bei einem zweiten Ausführungsbeispiel ist ein Zähler vorgesehen, der den Überlauf des Integrierergliedes überwacht und das Eingangssignal entsprechend gewichtet.

WO 01/24360 A1

FIG 1

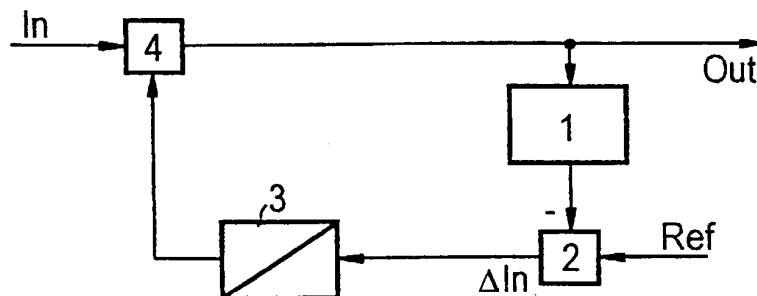


FIG 2

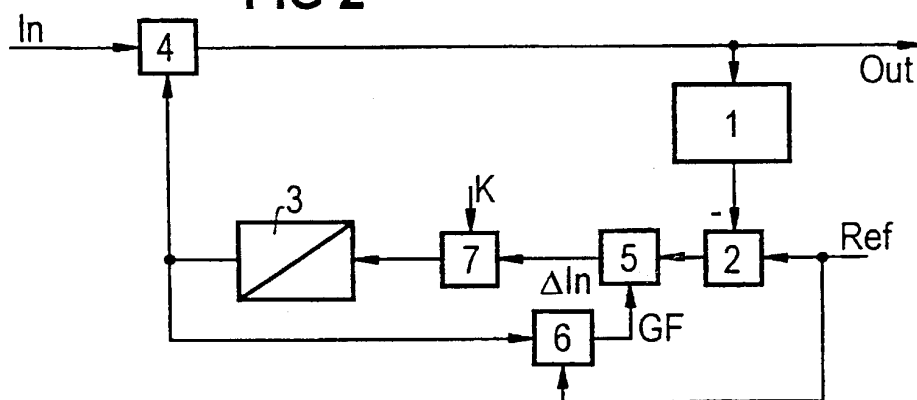
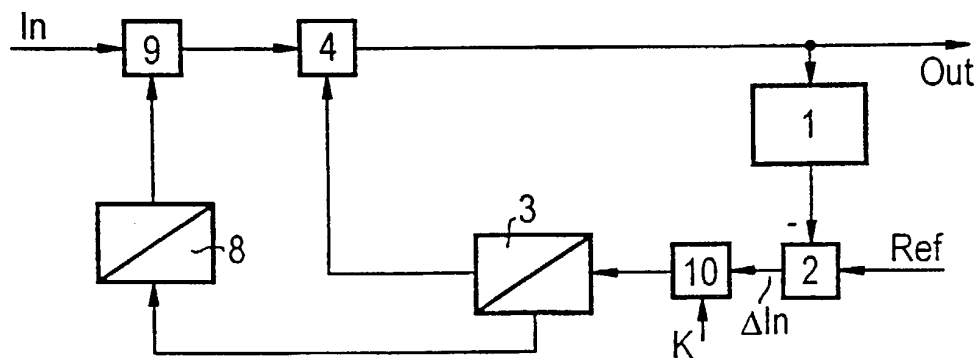


FIG 3





Micronas.6581

**DECLARATION AND POWER OF ATTORNEY**

I, the below named inventor, hereby declare that:

My residence, post office address, and citizenship are as stated below next to my name.

I believe I am the original, first, and sole inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled **CONTROL LOOP FOR DIGITAL SIGNALS** the specification which was filed with the United States Patent and Trademark Office on April 1, 2002 as Serial No. 10/089,654.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims.

I acknowledge the duty to disclose information which is material to patentability in accordance with Title 37, Code of Federal Regulations, Section 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code §119(a)-(d) or (f), or 365 (b) of any foreign application(s) for patent, inventor's or plant breeder's rights certificate(s), or 365 (a) of any PCT international application which designated at least one country other than the United States of America listed below and have also identified below any foreign application for patent, inventor's or plant breeder's rights certificate(s) filed by me on the same subject matter having a filing date before that of the application on which priority is claimed: International Patent Application No. PCT/EP00/09454 filed September 27, 2000.

I hereby declare that all statements are made hereby of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

And I hereby appoint:

Maurice E. Gauthier	-	Reg. No. <u>20,798</u>
Richard L. Stevens	-	Reg. No. <u>24,445</u>
Matthew E. Connors	-	Reg. No. <u>33,298</u>
William E. Hilton	-	Reg. No. <u>35,192</u>
Patrick J. O'Shea	-	Reg. No. <u>35,305</u>
Arlene J. Powers	-	Reg. No. <u>35,985</u>
Richard L. Stevens, Jr.	-	Reg. No. <u>44,357</u>
Peter Stecher	-	Reg. No. <u>47,259</u>

(8)

all of the firm of Samuels, Gauthier & Stevens, my attorneys with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith.

I request that all correspondence be directed to:

Patrick J. O'Shea, Esq.  
Samuels, Gauthier & Stevens, LLP  
225 Franklin Street, Suite 3300  
Boston, MA 02110

Andreas Menkhoff

15.5.02

/-00

Andreas Menkhoff

Date

Residence:

~~Hoeslstrasse 17~~ Auf dem Kyberg 24  
~~81927 Muenchen~~ 82041 Oberhaching  
 Germany

DEX

Citizenship

German

Post Office Address:

Same as above